IN THE SPECIFICATION

Please amend Page 16, Lines 13-18 as follows:

If any errors occur during verification of any of design stages 105-115, these errors are preferably corrected before going to a subsequent stage. At IC-assembly design stage [[108]] 120, the design process generates a top-level design for fabricating the desired circuit, as well as verifies test branches for each of the circuit blocks used in the design and the circuit as a whole.

Please amend Page 18, Lines 8-19 as follows:

Exemplary parser 235 is operable to translate the HDL description of the circuit to be simulated that is received from the circuit designer via interface 225. According to the illustrated embodiment, the HDL description of the circuit may suitably be translated into an expression tree conventionally commonly referred to as a Directed Acyclic Graph ("DAG"; DAGs may be directly derived from the HDL description of circuit elements, or, as in alternate implementations, may be derived first into an intermediate Register Transfer Level ("RTL") structure corresponding to the circuit elements and then into DAGs; further discussion of the same is beyond the scope of this patent document as it is well [[know]] known by those of skill in the art).